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Product Family	Product	Description	Function	Key Features/Benefits
ASICs	Application-Specific Integrated Circuits/System on Chip	Custom solutions for computing communications and consumer applications.	Speeds time to market with broad IP portfolio for customer IC solutions.	Lower cost per port, higher port densities, faster time to market.
ATM Access Processor	APC Family (APC, APC Ultra-Lite)	Single-chip OC-12 ATM solution.	Connection management, policing, traffic management, OAM.	Single-chip, complete ATM solution with a variety of price points. Software compatibility across all families.
ATM Access Processor	TAAD08JU2	Highly integrated device for ATM access (Layer 1 and Layer 2).	Provides QOS for a variety of ATM traffic types (on-chip APC). Support CBR, UBR, rt_VBR, nrt_VBR, and ABR. Provides AAL2/5 SAR for 2K CIDs/VC, integrated TC/IMA and framer for 8 T1/E1/J1s (PHY). Supports I.363.2 service, I.366.1 SSSAR service, I.366.1 SSTED service and I.363.5 CPCS service. Provides adaptation conversion of AAL5/AAL2 flows into AAL2/AAL5 flows (1300 flows). Maximum bandwidth = 155 Mbits/s through the SAR and APC. PHY bandwidth = 16 Mbits/s.	Unequaled HW/SW integration/density, no external memory required and price performance for target application provide low-cost system solution and fast time to market. Large number of flexible/modular interface ports provides multiple data paths for platform design.
ATM Access Processor	TAAD Lite	Low-speed ATM access solution.	T1/E1/J1 framing (8 links). ATM transmission convergence. Inverse multiplexing for ATM (T1/E1/J1). ATM switching and control. ATM adaptation layer (AAL2 & AAL5), AAL segmentation and reassembly (SAR).	High functional integration targeted to the wireless 3G radio access network, multiservice access platforms, and voice/multimedia gateways. Seamless, end-to-end multiservice hardware and applications software solutions. Highly flexible architectures. Flexible interfaces allow multiple/variable transport technologies to accommodate market requirements.
ATM Access Processor	TAAD UltraLite	Low-speed ATM access solution.	T1/E1/J1 framing (8 links). ATM transmission convergence. Inverse multiplexing for ATM (T1/E1/J1). ATM switching and control. ATM adaptation layer (AAL2 & AAL5), AAL segmentation and reassembly (SAR).	High functional integration targeted to the wireless 3G radio access network, multiservice access platforms and voice/multimedia gateways. Seamless, end-to-end multiservice hardware and applications software solutions. Highly flexible architectures. Flexible interfaces allows multiple/variable transport technologies to accommodate market requirements.
ATM Access Processor	SAR-500	Complete ATM adaptation solution.	Complete ATM adaptation solution. Implements any combination of 512 AAL2 CIDs/AAL5 VCs. Implements adaptation conversion of 512 AAL5/AAL2 flows into 512 AAL2/AAL5 flows.	Highly integrated ATM adaptation system on a chip + full-featured software + world-class support = fast time to market.
ATM Access Processor	SAR-1K	Complete ATM adaptation solution.	Complete ATM adaptation solution. Implements any combination of 1024 AAL2 CIDs/AAL5 VCs. Implements adaptation conversion of 1024 AAL5/AAL2 flows into 1024 AAL2/AAL5 flows.	Highly integrated ATM adaptation system on a chip + full-featured software + world-class support = fast time to market.

Product Family	Product	Description	Function	Key Features/Benefits
ATM Access Processor	SAR-2K	High-capacity device for ATM adaptation layer (AAL2 and AAL5).	Provides AAL2/5 SAR for 2K CIDs/VCs. Supports I.363.2 service, I.366.1 SSSAR service, I.366.1 SSTED service, and I.363.5 CPCS service. Provides adaptation conversion of AAL5/AAL2 flows into AAL2/AAL5 flows (1300 flows). Maximum bandwidth = 155 Mbits/s.	Full-featured ATM adaptation layer SoC, full-featured software, and no external memory required provide low-cost system solution.
ATM Interconnect	*CelXpres* T8207	Single-chip ATM switch and backplane I/F interconnecting UTOPIA Level 1/2 bus to a 1.7 Gbits/s ATM parallel cell bus backplane (OC-12 rate).	Performs cell routing between up to 32 line cards each supporting 32 MPHYs with 64 queues.	8-bit UTOPIA L1 and L2 I/F. 32 MPHY support. 64 queues available. VPI/VCI look-up and translation. 32-bit cell backplane with 66 MHz rate. Up to 32 devices supported on single bus.
ATM Interconnect	*CelXpres* T8208	Single-chip ATM switch and backplane I/F interconnecting UTOPIA Level 1/2 bus to a 1.7 Gbits/s ATM parallel cell bus backplane (OC-12 rate).	Performs cell routing between up to 32 line cards each supporting 64 MPHYs with 128 queues.	8-bit UTOPIA L1 and L2 I/F. 64 MPHY support. 128 queues available. VPI/VCI look-up and translation. 32-bit cell backplane with 66 MHz rate. Up to 32 devices supported on single bus.
Backplane Bridge	UBAPP500	POSPHYL3 protocol conversion engine to SONET SerDes. The UBAPP500 is IP code that can be loaded into the Lattice ORSO82G5 FPSC device.	Interconnects POSPHYL3 compliant devices to the PI40 fabric through 2.5G SerDes links. Seamlessly connects the APPxxx network processors to the PI40 fabric.	8/16/32-bit POSPHYL3 I/F. Support 256 MPHYs. Supports 72-byte cell size user payloads to PI40. Eight pseudo SONET SerDes links operating at 2.5 Gbits/s. Packet extraction port. 8-bit asynchronous µP I/F.
Backplane Bridge	UBAPC	APC conversion engine to SONET SerDes. The UBAPC is IP code that can be loaded into the Lattice ORSO82G5 FPSC device.	Seamlessly connects two APC devices to the PI40 fabric through 2.5G SerDes links.	Two 8-bit APC ATM I/F. Supports 72-byte cell size user payloads to PI40. Four pseudo SONET SerDes links operating at 2.5 Gbits/s. 8-bit asynchronous µP I/F.
Backplane Bridge	UBCSIX	CSIX L1 protocol conversion engine to SONET SerDes. The UBCSIX is IP code that can be loaded into the Lattice ORSO82G5 FPSC device.	Interconnects CSIX L1 compliant devices to the PI40 fabric through 2.5G SerDes links. Seamlessly connects the *Motorola*® C5E and the *Intel*® IXP2400 network processors to the PI40 fabric.	32-bit CSIX L1 fabric I/F. Supports 1024 ports, Four traffic classes. Supports 72-byte cell size user payloads to PI40. Four pseudo SONET SerDes links operating at 2.5 Gbits/s. 8-bit asynchronous µP I/F.
Backplane Transceiver	TTSV04622	SONET/SDH compliant OC-48/4x OC-12 low-cost backplane transceiver.	SONET/SDH backplane transceiver supports OC-48/4x OC-12 and telecom bus 77 MHz TTL byte wide on line side.	1xOC-48, 4x OC-12, and telecom bus 77 MHz. Applications: can be used for low-speed interface or together with TADM.
Backplane Transceiver	TTSV02622	SONET/SDH compliant OC-48/2x OC-12 low-cost backplane transceiver.	SONET/SDH backplane transceiver supports OC-48/2x OC-12 and telecom bus 77 MHz TTL byte wide on line side.	1xOC-48, 2x OC-12, and telecom bus 77 MHz. Applications: can be used for low-speed interface or together with TADM.

Product Family	Product	Description	Function	Key Features/Benefits
Clock Driver	LCK4011	Programmable clock synthesizer.	A PLL-based clock driver targeted at stackable computing/ datacom applications; SAN (storage area network), storage media devices, and HBA (host bus adapter).	Uses a single crystal oscillator to generate all output frequencies. Four interconnected programmable PLLs ultimately enabling output frequencies ranging from 3.125 MHz to 400 MHz. Output multiplexer array can direct numerous output frequencies to 24 output ports. Phase delay compensation is available on 6 outputs. Output buffer types include 1.2 V, 1.5 V, 2.5 V, and 3.3 V single ended as well as LVDS. Output can be stopped (either high or low, depending on port).
Clock Driver	LCK4012	High-speed programmable clock synthesizer.	A PLL-based clock driver targeted at stackable computing/ datacom applications; SAN (storage area network), storage media devices, and HBA (host bus adapter).	All features of the LCK4011. Four interconnected programmable PLLs ultimately enabling output frequencies ranging from 3.125 MHz to 800 MHz.
Clock Driver	LCK4013	High-speed programmable clock synthesizer with spread spectrum capability.	A PLL-based clock driver targeted at PC motherboard, hand-held device, PDA, PC peripherals, printers, copiers, FAXes, SAN (storage area network), storage media devices, and HBA (host bus adapter).	All features of the LCK4012. Three of the output PLLs support spread spectrum generation capability. One of the output PLLs supports frequency slewing capability to smoothly change the output frequency (e.g., low-power clock mode).
Clock Driver	LCK4953	Low-voltage PLL clock driver.	A PLL-based clock driver targeted at high-end computer workstations and network servers.	Output frequencies to 130 MHz in PLL mode; pin compatible with MPC953 types; low jitter, 50 ps cycle-to-cycle; low output-to-output skew of 75 ps; nine outputs with high-impedance disable; zero delay performance; 3.3 V system compatibility; no external loop filter components needed; 32-lead TQFP.
Clock Driver	LCK4972	Low-voltage PLL clock driver.	A 3.3 V and 2.5 V PLL-based clock driver for high-performance RISC or CISC processor based system.	Fully integrated PLL; output frequency up to 240 MHz; selectable one crystal input or two single- ended TTI inputs; pin compatible with MPC972 types; compatible with *PowerPC*™ and *Pentium*® microprocessors; 52-pin LQFP; 3.3 V & 2.5 V power supply; 100 ps typical cycle-to-cycle jitter; low output-to-output skew of 250 ps.
Cross Connect	TDCS4810G	10G STS cross connect.	10G aggregate bandwidth nonblocking STS-1/STM-1 granularity switch with 48 channels.	Nonblocking; TDM circuit grooming cross connect; migration path from TADM to stand-alone/cascadable 40G TDM switch; enables higher bandwidth and ADM ring support at OC192 and greater. Software drivers available for reducing design time.
Cross Connect	TDCS6440G	40G cross connect.	40G aggregate bandwidth non-blocking STS-1/STM-1 granularity switch.	Nonblocking; TDM circuit grooming cross connect; migration path from TADM to stand-alone/cascadable 40G TDM switch; enables higher bandwidth and ADM ring support at OC192 and greater. Software drivers available for reducing design time.
DSP	DSP16410	High-performance digital signal processor (DSP), two DSP16000 DSP cores, 780 MMACS, 3 Mbits on-board memory.	Equalization and channel processing in 2G/2.5G wireless base stations. Multichannel speech processing in voice gateways.	Twin DSP16000 dual-MAC cores. Small package, low power consumption.

Product Family	Product	Description	Function	Key Features/Benefits
DSP	DSP16411	High-performance digital signal processor (DSP), two DSP16000 DSP cores, 1140 MMACS, 5 Mbits on-board memory.	Equalization and channel processing in 2G/2.5G wireless base stations. Multichannel speech processing in voice gateways.	Performance improvement/cost reduction versus DSP16410, software compatible, higher maximum clock rate, and increased memory.
Framer	MARS10G T-Uni (TSOT1610G)	16xSTS-3/12, 4xSTS48, or 1xSTS192 SONET/SDH framer.	Supports 16 STS-3/12, 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G TD-Uni (TSOT1610GD)	16xSTS-3/12, 4xSTS48, or 1xSTS192 SONET/SDH framer.	Supports 16 STS-3/12, 4xSTS-48, or 1xSTS192 SONET/SDH with a 16-channel framer with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Applications: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G T-Pro (TSOT1610GP)	4xSTS48 or 1xSTS192 SONET/SDH framer.	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G TD-Pro (TSOT1610GPD)	4xSTS48 or 1xSTS192 SONET/SDH framer.	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Applications: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G T-Pro16 (TSOT1610GP6)	16xSTS-3 or 16xSTS-12 SONET/SDH framer.	Supports 16 STS-3/12 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G TD-Pro16 (TSOT1610GP6D)	16xSTS-3 or 16xSTS-12 SONET/SDH framer.	Supports 16 STS-3/12 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Applications: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS5G T-Pro16 (TSOT1605GP6)	16xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer.	Supports 16 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency, and optional 2.5G backplane interface.	Highly integrated, extremely versatile 5G framer with integrated cross-connect support, and price competitive. Applications: POS, ATM, TDM data handle. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS5G T-Pro8 (TSOT1605GP8)	8xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer.	Supports 8 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile 5G framer with integrated cross-connect support, and price competitive. Access applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS2G5 T-Pro16 (TSOT162G5P6)	16xSTS-3, 4xSTS-12, 1xSTS48 SONET/SDH framer.	Supports 16xSTS-3, 4xSTS-12, 1xSTS-48 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Access applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.

Product Family	Product	Description	Function	Key Features/Benefits
Framer	MARS2G5 TD-Pro16 (TSOT162D5P6)	16xSTS-3, 4xSTS-12, 1xSTS48 SONET/SDH framer.	Supports 16xSTS-3, 4xSTS-12, 1xSTS-48 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Access application: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G T-UniPHY (TSOT1610GA)	16xSTS-3/12, 4xSTS48, or 1xSTS192 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16 STS-3/12, 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross connect support, tandem connection maintenance (TCM), bit-slice support on the 2.5 Gbits/s backplane, TOH transparency support for DWDM aggregator, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G TD-UniPHY (TSOT1610GAD)	16xSTS-3/12, 4xSTS48, or 1xSTS192 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16 STS-3/12, 4xSTS-48, or 1xSTS192 SONET/SDH with a 16-channel framer with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Application: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G T-ProPHY (TSOT1610GAP)	4xSTS48 or 1xSTS192 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross-connect support, tandem connection maintenance (TCM), bit-slice support on the 2.5 Gbits/s backplane, TOH transparency support for DWDM aggregator, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G TD-ProPHY (TSOT1610GAPD)	4xSTS48 or 1xSTS192 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Application: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G T-Pro16PHY (TSOT1610GAP6)	16xSTS-3 or 16xSTS-12 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16 STS-3/12 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile with integrated cross-connect support, tandem connection maintenance (TCM), bit-slice support on the 2.5 Gbits/s backplane, TOH transparency support for DWDM aggregator, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS10G TD-Pro16PHY (TSOT1610GAP6D)	16xSTS-3 or 16xSTS-12 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16 STS-3/12 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Application: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS5G T-Pro16PHY (TSOT1605GAP6)	16xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency, and optional 2.5G backplane interface.	Highly integrated, extremely versatile 5G framer with integrated cross-connect support, tandem connection maintenance (TCM), bit-slice support on the 2.5 Gbits/s backplane, TOH transparency support for DWDM aggregator, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.

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Framer	MARS5G T-Pro8PHY (TSOT1605GAP8)	8xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 8 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile 5G framer with integrated cross-connect support, tandem connection maintenance (TCM), bit-slice support on the 2.5 Gbits/s backplane, TOH transparency support for DWDM aggregator, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS2G5 T-Pro16PHY (TSOT162G5AP6)	16xSTS-3, 4xSTS-12, or 1xSTS48 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16xSTS-3, 4xSTS-12, 1xSTS-48 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5G/622 MHz backplane interface.	Highly integrated, extremely versatile 5G framer with integrated cross-connect support, tandem connection maintenance (TCM), bit-slice support on the 2.5 Gbits/s backplane, TOH transparency support for DWDM aggregator, and price competitive. Applications: ADM, MSPP, etc. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS2G5 TD-Pro16PHY (TSOT162D5AP6)	16xSTS-3, 4xSTS-12, or 1xSTS48 SONET/SDH framer. Integrated multirate CDR support autorate detection from STS-3/12 and STS-48.	Supports 16xSTS-3, 4xSTS-12, 1xSTS-48 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile with integrated cross-connect support, and price competitive. Access application: DWDM. Available software drivers are reusable across multiple devices for reducing design time.
Framer	MARS2G5 T (TSOTLT2G5)	STS-3/12/48 SONET/SDH framer.	4xSTS-3/12 or 1xSTS48 SONET/SDH framer with APS support, and cross connect.	Highly integrated, extremely versatile with 12.5G integrated cross-connect, proven technology, and price competitive. Software drivers available for reducing design time.
Framer	MARS622 T (TSOT04622)	STS-3/12 SONET/SDH framer.	4xSTS-3 or 1xSTS12 SONET/SDH framer with APS support, and cross connect.	Extremely versatile, proven technology, with 12.5G integrated cross-connect, and price competitive. Access applications: ADM, MSPP, etc. Software drivers available for reducing design time.
Framer	MARS2G5 T-LT (TSOT042G5)	STS-3/12/48 SONET/SDH framer.	Latest version TSOT with 1.6 V core. This device supports 4xSTS-3/12 or 1xSTS48 SONET/SDH framer with APS support, and cross connect.	Highly integrated, extremely versatile with 12.5G integrated cross-connect, proven technology, and price competitive. Access applications: ADM, MSPP, etc. Software drivers available for reducing design time.
Framer	MARS2G5 P-VC ULM *Datamapper*™ (TDM2G5ULM))	Ethernet over SONET/SDH solution with traffic manager.	Maps Ethernet/IP data over SONET/SDH with GFP/HDLC and VC/LCAS. Has integrated traffic management with policing, buffering, and scheduling.	More efficient use of network resources due to the oversubscription capabilities. Integrated Ethernet MACS and clock data recovery reduces device count of solution.
Framer	MARS2G5 P-VC (TADMVC2G52)	STS-3/12/48 SONET/SDH ADM with ATM and/or packet data engine and virtual concatenation.	The TADMVC2G5 P-VC is a low-power device with 1.6 V core and enhanced data engine capabilities including high-order virtual concatenation, with limited GFP-F support. Supports 4xSTS-3, or 4xSTS12, or 1xSTS48 SONET/SDH/POF/POS with a 16-channel framer. APS, cross connect, and enhanced data engine.	Highly integrated, extremely versatile with 12.5G integrated cross-connect support, high-order (STS) virtual concatenation with LCAS, proven technology, and price competitive. Applications: POS, ATM, HDLS/PPP, GeOS, and IP.

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Framer	MARS1G2 P-VC (TADMVC1G2)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine and virtual concatenation.	The TADMVC1G2 P-VC is a low-power device with 1.6 V core and enhanced data engine capabilities including high-order virtual concatenation. 792-pin PBGA packages. Supports 4xSTS-3, or 2xSTS12 SONET/SDH/POF/POS with a 16-channel framer including APS, cross connect, and enhanced data engine.	Highly integrated, extremely versatile with 12.5G integrated cross-connect support, high-order (STS) virtual concatenation with LCAS, proven technology, and price competitive. Applications: POS, ATM, HDLS/PPP, GeOS, and IP. Software drivers available for reducing design time.
Framer	MARS622 P-VC (TADMVC622)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine and virtual concatenation.	The TADMVC1G2 P-VC is a low-power device with 1.6 V core and enhanced data engine capabilities including high-order virtual concatenation. Supports 4xSTS-3, or 1xSTS12 SONET/SDH/POF/POS with a 16-channel framer including APS, cross connect, and enhanced data engine.	Highly integrated, extremely versatile with 12.5G integrated cross-connect support, high-order (STS) virtual concatenation with LCAS, proven technology, and price competitive. Applications: POS, ATM, HDLS/PPP, GeOS, and IP. Software drivers available for reducing design time.
Framer	MARS1G2 P (TADM021G2)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine.	4xSTS-3, 2xSTS-12 SONET/SDH, or POF/POS 16-channel framer with APS, cross connect, and data engine.	Highly integrated, proven technology, and price competitive.
Framer	MARS622P (TADM04622)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine.	4xSTS-3, 2xSTS-12 SONET/SDH, or POF/POS 16-channel framer with APS, cross connect, and data engine.	Highly integrated, proven technology, and price competitive.
Framer	MARS2G5 P (TADM042G52)	STS-3/12/48 SONET/SDH ADM with ATM and/or packet data engine.	4xSTS-3, 4xSTS-12, or 1xSTS-48 SONET/SDH or POF/POS 16-channel framer with APS, cross connect, and data engine.	Highly integrated, proven technology, and price competitive.
Framer	MARS2G5 P-MaxLT (TSDE162G52)	2.5G 16-channel data engine.	The TADM2G5 P-MaxLT is a low-power device with 1.6 V core and enhanced data engine capabilities. Support 16-channel framer, GFP-F. Terminates ATM, HDLC, and DS3.	Highly integrated, extremely versatile with 12.5G integrated cross connect, proven technology, and price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS1G2 P-LT (TDAT161G2)	16-channel data engine.	4xSTS-3 or 2xSTS-12 SONET/SDH four-channel framer with ATM path processing in data engine. Terminate ATM, HDLC, and DS3.	Highly integrated, proven technology, and price competitive. Supports ATM, HDLC, DS3 termination. Application: DSLAM.
Framer	MARS622 P-LT (TDAT12622)	SONET/SDH framer combined with a 12-channel data engine.	4xSTS-3 or 1xSTS-12 SONET/SDH four-channel framer with ATM path processing in data engine. Terminate ATM, HDLC, and DS3.	Highly integrated, proven technology, and price competitive. Supports ATM, HDLC, DS3 termination. Application: DSLAM.
Framer	MARS2G5 P-Pro (TDAT162G52)	SONET/SDH framer combined with a 16-channel data engine.	4xOC-3, or 4xOC12, or 1xOC-48 SONET/SDH 16-channel framer with ATM path processing in data engine.	Highly integrated, extremely versatile, proven technology, and price competitive. Supports ATM, HDLC, DS3 termination. Application: DSLAM.
Framer	MARS2G5 P-ProLT (TDAT042G52LT)	SONET/SDH framer combined with a four-channel data engine.	4xOC-3, or 4xOC12, or 1xOC-48 SONET/SDH four-channel framer with ATM path processing in data engine.	Highly integrated, proven technology, and price competitive. Application: DSLAM.

Product Family	Product	Description	Function	Key Features/Benefits
Framer	MARS622 P-ProLT (TDAT04622LT)	STS-12 SONET/SDH with ATM and a four-channel data engine.	STS-3/12 SONET/SDH interface with ATM data engine. 4xSTS-12 SONET/SDH four-channel framer with ATM path processing in data engine.	Highly integrated, proven technology, and price competitive.
Framer (T1/E1/J1)	Superframer (TFRA28J133)	T1/E1/J1 framer used in OC1 to OC3 applications.	Used in DS3, DS2, T1/E1/J1, and DS0/E0 applications.	Alarm reporting and performance monitoring per *AT&T* ™, *ANSI* ®, ITU-T, ETSI, and Japanese standards. Flexible PDH interfaces.
Framer (T1/E1/J1)	Ultraframer (TFRA84J131)	T1/E1/J1 framer used in OC3 to OC12 applications.	Used in DS3/E3, DS2, T1/E1/J1, and DS0/E0 applications.	Alarm reporting and performance monitoring per *AT&T, ANSI*, ITU-T, ETSI, and Japanese standards. Flexible PDH interfaces.
Gigabit Ethernet Switch	ET4K Gigabit Ethernet L2 Switches	The ET4K is a new generation of Gigabit Ethernet switch chips. It is a true switch-on-a-chip product family that integrates all switch functions on a single silicon device. It provides the highest integration level in industry. Coupled with Agere's ET1081 Octal PHY devices, the Agere Gigabit Ethernet switching solution enables the low cost and power implementation of enterprise switches at 10/100/1000 Mbits/s Ethernet speeds.	L2 switching with L2/L3/L4 QoS and ACL capability. • ET4101 - 48 10/100/1000 Mbits/s SGMII ports, 4 Gigabit SerDes ports, 2 10G XAUI ports. • ET4001 - 48 10/100/1000 Mbits/s SGMII ports, 4 Gigabit SerDes ports. • ET4100 - 24 10/100/1000 Mbits/s SGMII ports, 4 Gigabit SerDes ports, 2 10G XAUI ports. • ET4000 - 24 10/100/1000 Mbits/s SGMII ports, 4 Gigabit SerDes ports.	Wire speed performance - wire speed L2 bridging and L2/L3/L4 classification, 8K MAC addresses, L2/L3/L4 access control list, IPv4 and IPv6, 256 VLANs, 802.3x flow control, 802.1p CoS, L3 DSCP, traffic policing, traffic shaping and scheduling, 8 class queues per port, boardcast and multicast storm control, link aggregation, multiple spanning trees, integrated 10G MACs for uplink or stacking, PCI host interface, 6-layer board PCB implementation.
Gigabit Ethernet Transceiver	*TruePHY*™ ET1011	10Base-T, 100Base-Tx, and 1000Base-T Gigabit Ethernet transceivers.	Single CMOS chip in a 128-pin TQFP or 68-pin MLCC for 10Base-T, 100Base-T, and 1000Base-T Gigabit Ethernet applications. Designed for low-cost and low-power applications in server, desktop NIC/LOM cards, VoIP, IP-DSLAM, test equipment, networking printers, storages, and consumer applications.	Fully compliant with 802.3, 802.3a, and 802.3ab standards. Includes RGMII, GMII, MII, RTBI, and TBI interfaces to MAC or switch. Lower power consumption: <750 mW in 1000Base-T mode. Advanced power management. Uses oversampling for implementing a fractionally spaced equalizer, which provides better equalization and has greater immunity to timing jitter, resulting in better signal-to-noise ratio (SNR) and thus improved BER.
Gigabit Ethernet Transceiver	*TruePHY* ET1081	Octal 1000Base-T Gigabit Ethernet transceiver.	Octal Gigabit Ethernet transceiver for Ethernet switching applications. Designed in TSMC 0.13 µm technology. Enables high-density line card design.	Low-power architecture simplifies line card design and thermal management. At less than 750 mW per port in 1000Base-T mode including all interface and I/O power, the ET1081 is the industry's lowest-power octal PHY. The ET1081 is in a low-cost 388-PBGA package. The integration of 8 PHY ports in one die and the low pin count SGMII MAC interfaces reduces board-level component count and reduces the number of PCB traces, which simplifies board routing, PCB design, and thermal management.

Product Family	Product	Description	Function	Key Features/Benefits
Gigabit Ethernet Transceiver	*TruePHY* ET1310 *PCI Express*™ Gigabit Ethernet MAC/PHY Controller	The ET1310-type is a new generation of Gigabit Ethernet controllers that provide the combination of performance, power, and cost attributes that enable migration to Gigabit Ethernet for all mainstream NIC/LOM desktop and notebook applications.	Provides a complete single-chip Gigabit Ethernet MAC/PHY controller that is designed from the ground up for the advanced performance, concurrency, and power management capabilities of *PCI Express*.	Higher performance — full rate throughput without PCI bottleneck. Native *PCI Express* device architecture of the ET1310 enables the full suite of performance benefits of *PCI Express*. Lower power — lower total power due to reduced on-chip memory and extensive use of *PCI Express* active state power management to minimize dynamic power. Full mode power consumption is less than 900 mW, with approximately 20 mW in standby. Small footprint and advanced packaging — the ET1310 features an ultrasmall 10 mm x 10 mm, 68-pin MLCC package that is offered for both Pb-free and traditional manufacturing environments. Commercial and industrial temperature ranges are available. Higher system reliability — full support of *PCI Express* active error reporting features. A full suite of software support enables a smooth transition to *PCI Express* as the industry-standard host interface.
HDLC Controller	Link Layer Processor	Medium-capacity, high-level data link controller (HDLC) with multilink PPP. Includes 16-channel T1/E1 framer.	Provides high-level data link controller (HDLC) for 672 channels. Also includes multilink PPP capability with up to 84 T1 links and 63 E1 links. Maximum bandwidth = 155 Mbits/s.	Allows customers to migrate from current ATM solutions to newer IP-based solutions. Full-featured software.
IEEE 1394	FW322 06	Two-port, PCI-based 1394A open host controller interface (OHCI) link-layer controller and physical layer (PHY).	Provides a single-chip solution for connecting two *IEEE* 1394A cable ports to a host system using the PCI bus and OHCI 1.2.	OHCI link-layer controller and PHY in a single package. Supports two fully compliant cable ports, each running at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. Compliant with 1394A-2000, 1394-1995, OHCI 1.2, PCI 2.2, and PCI power management interface 1.1. Serial EEPROM interface for storing configuration data. 3.3 V operation, 5 V tolerant inputs. 120-pin TQFP package.
IEEE 1394	FW323 06	Three-port, PCI-based 1394A open host controller interface (OHCI) link-layer controller and physical layer (PHY).	Provides a single-chip solution for connecting three *IEEE* 1394A cable ports to a host system using the PCI bus and OHCI 1.2.	OHCI link-layer controller and PHY in a single package. Supports three fully compliant cable ports, each running at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. Compliant with 1394A-2000, 1394-1995, OHCI 1.2, PCI 2.2, and PCI power management interface 1.1. Serial EEPROM interface for storing configuration data. 3.3 V operation, 5 V tolerant inputs. 128-pin TQFP package.
IEEE 1394	FW801A FW801BF	One-port *IEEE* 1394A-2000 cable transceiver/arbiter.	Provides the analog physical layer functions needed to implement one cable port in an *IEEE* 1394-1995 or *IEEE* 1394A-2000 network. This device interfaces to a separate link-layer controller through a 2/4/8 line parallel interface at 50 Mbits/s.	Provides one fully compliant cable port at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. Compliant with *IEEE* 1394A-2000 and *IEEE* 1394-1995. Fully supports open HCI requirements. Data interface to link-layer controller provided through 2/4/8 parallel lines at 50 Mbits/s. Single 3.3 V supply operation. Package: FW801A—48-pin TQFP, FW801BF—48-pin TFSBGA.

Product Family	Product	Description	Function	Key Features/Benefits
IEEE 1394	FW802B FW802C FW802BF	Two-port *IEEE* 1394A-2000 cable transceiver/ arbiter.	Provides the analog physical layer functions needed to implement two cable ports in an *IEEE* 1394-1995 or *IEEE* 1394A-2000 network. This device interfaces to a separate link-layer controller through a 2/4/8 line parallel interface at 50 Mbits/s.	Provides two fully compliant cable ports at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. Compliant with *IEEE* 1394A-2000 and *IEEE* 1394-1995. Fully supports open HCI requirements. Data interface to link-layer controller provided through 2/4/8 parallel lines at 50 Mbits/s. Single 3.3 V supply operation. Package: FW802B—64-pin TQFP, FW802C—48-pin TQFP, FW802BF—48-pin TFSBGA.
Lithium-Ion Battery Charger Controller	PSC1534	Lithium-Ion (Li-Ion) battery charger controller. Appropriate for any application that requires a compact, low-cost solution.	A constant-current, constant-voltage solution that allows charge current programming using a single external resistor (RPROG). Functional and performance equivalent to Linear Technologies LTC 1734. Typical applications include cell phones, PDAs, portable MP3 players, and other portable devices that use rechargeable Li-Ion batteries.	Very price competitive. Low external component count and small footprint. Charge termination indication and manual shutdown using PROG pin. Programmable charge current: 200 mA to 800 mA. 4.1 V or 4.2 V preset voltages. Automatic trickle charging for heavily discharged batteries requires no additional external components. Very low quiescent battery current during shutdown and standby (charger removed). Charger undervoltage lockout and battery overvoltage lockout. Overcurrent protection. Overtemperature protection. Low-profile (1 mm) 6-lead plastic SOT-23 package.
Mapper	*Hypermapper*™ (TMXF33625)	Integrated SONET/SDH mapper, MUX, and T1/E1/J1 framer. Used for OC3 or OC12 applications.	622/155 Mbit/s SONET/SDH interface for DS3, E3, DS2, DS1, E1 and DS0/E0 applications. Supports 1:1 and 1 + 1 protection schemes.	Extremely versatile device with tremendous integration and flexibility. Can be used in numerous applications. Supports ITU, *Telcordia Technologies®, ANSI*, and Japanese standards.
Mapper	*Supermapper*™ (TMXF28155)	Integrated SONET/SDH mapper, MUX, and T1/E1/J1 framer. Used for OC3 or STS1/STM0.	155/51 Mbits/s SONET/SDH interface for DS3, DS2, DS1, E1, J1, and DS0/E0 applications. Supports 1 + 1 and ring protection with additional devices.	Extremely versatile device with tremendous integration and flexibility. Can be used in numerous applications. Supports ITU, *Telcordia Technologies, ANSI, ETSI*, and Japanese standards.
Mapper	*Ultramapper*™ (TMXF84622)	Integrated SONET/SDH mapper, MUX, and T1/E1/J1 framer. Used for OC3 or OC12 applications.	622/155 Mbits/s SONET/SDH interface for DS3, E3, DS2, DS1, E1, J1, and DS0/E0 applications. Supports 1 + 1 and ring protection with additional devices.	Extremely versatile device with tremendous integration and flexibility. Can be used in numerous applications. Supports ITU, *Telcordia Technologies, ANSI*, and Japanese standards.
Mobile Handset Solutions - UMTS/EDGE/GPRS/ GSM *Vision*™	*Vision* Chip Set and Software Stack	Mobile handset architecture that enables phone manufacturers to more rapidly deliver a broad portfolio of products aimed at addressing the growing demand for multimedia capable wireless phones supporting real-time audio and video streaming, digital photo imaging, and interactive gaming.	The architecture includes a digital baseband chip set that uses a low-leakage process technology and multiple processors, enabling key enhancements in security, performance, and power management.	Flexible multicore hardware architecture delivers mobile multimedia. Strength and scalability from decoupled applications and communications processors: quicker product spins and faster time to volume. Unique software architecture: proven protocol stack, assured communication environment, open and proprietary OS support, *OptiSuite*™ design tools. Uncompromising mobility: three separate processor domains deliver performance and power efficiencies, lower BOM, smaller size, lower component count. Capable of providing 50 percent longer battery life than comparable single processor multimedia solutions.

Product Family	Product	Description	Function	Key Features/Benefits
Mobile Handset Solutions - UMTS/EDGE/GPRS/GSM *Sceptre*®	*Sceptre* HPU Chip Set and Software Stack	Three-chip solution incorporating proven Sceptre HPE EDGE Class 12 chip set and programmable UMTS baseband processor supporting release 99. Rapid, low-risk development and production of high-performance 3G handsets can be realized with Sceptre HPU integrated chip set and software solution. Unlike other 3G offerings, Sceptre HPU is an integrated quad protocol W-EDGE silicon and software solution, providing seamless access to UMTS, EDGE, GPRS, and GSM networks.	Broadband cellular access to 3G and 2.5G networks, combining data rates of up to 384 Kbits/s (UMTS) with up to 220 Kbits/s (EDGE) delivering automatic handovers between UMTS, EDGE, and GPRS.	*Sceptre* HPU is scalable for entry to mid- and high-end 3G solutions and provides proven interfaces designed to work with multimedia coprocessors and applications processors. As a stand-alone solution, *Sceptre* HPU's advanced multimedia support includes dynamic loudness adjustment, full-duplex speakerphone, HiFi audio routing, PCM audio interface, integrated polyphonic emulation: 40+ voices, MP2, and AAC decode. The solution supports a high level of video performance without the need of a coprocessor including MPEG4 playback at QCIF 18 frames per second and MPEG record at QCIF 10 frames per second. Higher levels of multimedia such as MPEG4 VGA video as well as video telephony are supported through an external multimedia accelerator or applications processor.
Mobile Handset Solutions - EDGE/GPRS/GSM *Sceptre*	*Sceptre* HPE Chip Set and Software Stack	High-performance hardware and software GSM/GPRS baseband solution for GPRS Class 12 mobile terminals. Includes a powerful *ARM* 946 microprocessor core that enables mobile phones with advanced, high-speed multimedia and entertainment applications. This system is offered as a complete circuit board-level hardware and software reference platform, including integrated silicon, software stack, and validated applications.	Industry's smallest and fastest EDGE silicon solution for high-speed enhanced mobile terminal designs. Pin compatible with *Sceptre* HP.	A high level of H/W and S/W integration delivers a 164 mm^2 chip set for smaller reference designs and more compact handsets. Delivers over 200 kbits/s download speed—four times faster than most fixed PC dial-up connections and upload speeds that exceed 100 kbits/s. Proven solution via extensive IOT testing. Provides extended battery time for three hours of talk time and 600 hours of standby time augmented by a highly optimized solution allowing slower clock speeds and reduced current leakage. Supports quadband operation (850 MHz, 900 MHz, 1800 MHz, 1900 MHz) and voice HR/FR/EFR/AMR, all with voice tags as well as advanced connectivity support for SD/MMC, USB, *Bluetooth*™, IrDA, and others. This solution is Class 12 capable. This high-performance solution provides all of the power needed to handle wireless communications and applications processing without the need for a separate applications processor.
Mobile Handset Solutions - EDGE/GPRS/GSM *Sceptre*	*Sceptre* HP Chip Set and Software Stack	High-performance hardware and software GSM/GPRS baseband solution for GPRS Class 12 mobile terminals. Includes a powerful *ARM* 946 microprocessor core that enables mobile phones with advanced, high-speed multimedia and entertainment applications. This system is offered as a complete circuit board-level hardware and software reference platform, including integrated silicon, software stack, and validated applications.	Hardware consists of a two-chip set: TRHP includes a DSP16000 and *ARM* 946E-S, both running at 90 MHz, and the CSP2200 mixed-signal device provides the interface function between TRHP and the RF subsystem as well as voice codecs and power management functions. Chip set is compatible with industry-leading third-party RF transceivers. DSP and MCU protocol stack software provide all communications system functionality. Pin compatible with *Sceptre* HPE.	GSM/GPRS Class 10 (Class 12 capable) baseband solution. Supports quad band operation (850 MHz, 900 MHz, 1800 MHz, 1900 MHz). Supports GPRS network modes 1, 2, 3. Advanced connectivity options, including an on-chip USB controller, IrDA, removeable secure digital (SD) and multimedia memory cards (MMC) and *Bluetooth*™ support. Integrated linear battery charger. Circuit-switched data (CSD) up to 14.4 Kbytes/s (data and FAX). CPHS V4.2. 164 mm2 chip set footprint. Triple-rate voice codecs with FR/EFR/HR or FR/EFR/AMR, all with AMR voice tags. Very low power consumption. This high-performance solution provides all of the power needed to handle wireless communications and applications processing without the need for a separate applications processor.

Product Family	Product	Description	Function	Key Features/Benefits
Mobile Handset Solutions - EDGE/GPRS/GSM *Sceptre*	Sceptre TC Chip Set and Software Stack	Complete two-chip GSM/GPRS baseband solution for GPRS Class 12 mobile terminals. Reduces three-chip Sceptre LF chip set into two chips. This system is offered as a complete circuit board-level hardware and software reference platform, including integrated silicon, software stack, and validated applications.	Hardware consists of a two-chip set; the TR09 DSP16000/ARM7TDMI dual processor, and the CSP2200 mixed-signal device provides the interface function between TR09 and the RF subsystem as well as the power management functions. Chip set is compatible with industry-leading third-party RF transceivers. DSP and MCU protocol stack software provide all communications system functionality.	GSM/GPRS Class 12 capable baseband solution. Class 10 provided, certified to GCF 3.9.0. Supports quad band operation (850 MHz, 900 MHz, 1800 MHz, 1900 MHz). Supports GPRS network modes 1, 2, 3. Integrated linear battery charger. Circuit-switched data (CSD) up to 14.4 Kbytes/s (data and FAX). EOTD phase 1 & 2 location support. 145 mm_ chip set footprint. Triple-rate voice codecs with FR/EFR/HR or FR/EFR/AMR, all with AMR voice tags. Very low power consumptio
Mobile Handset Solutions - EDGE/GPRS/GSM *Sceptre*	*Sceptre* LF Chip Set and Software Stack	Complete three-chip GSM/GPRS baseband solution for GPRS Class 12 mobile terminals.	Hardware consists of a three-chip set; TR09 DSP16000/ARM7TDMI dual processor, CSP1093C mixed-signal device provides the interface function between Trident II and the RF subsystem, and the PSC2106 integrated power management controller. Chip set is compatible with industry-leading third-party RF transceivers. DSP and MCU protocol stack software provide all communications system functionality.	GSM/GPRS Class 12 capable baseband solution. Class 10 provided, certified to GCF 3.9.0. Supports quad band operation (850 MHz, 900 MHz, 1800 MHz, 1900 MHz). Supports GPRS network modes 1, 2, 3. Circuit-switched data (CSD) up to 14.4 Kbytes/s (data and FAX). EOTD Phase 1 & 2 location support. 209 mm_ chip set footprint. Triple-rate voice codecs with FR/EFR/HR or FR/EFR/AMR all with AMR voice tags. Very low power consumption.
Modem - Codec	CSP1034AH (5 Volt) CSP1034C (3 Volt) CSP1034S (3 Volt)	Line codec for use with Agere's modem chip sets utilizing a transformer-based DAA (data access arrangement).	Provides analog signal filtering along with D/A and A/D conversions. Uses a transformer as the isolation barrier between the high-voltage phone line and the low-voltage modem DSP.	48-pin TQFP or 44-pin MQFP with built-in caller-ID circuitry. CSP1034C also in 44-pin MQFP. CSP1034S in 48-pin TQFP and 38-pin TTSOP. CSP1034S' D/A user amplifier can be tristated under software control. Benefit: reduce the op-amp output loading on the line during snoop modes.
Modem - Codec	CSP1035A (3 Volt)	Line codec for use with Agere's modem chip sets not using a transformer-based DAA.	Provides analog signal filtering along with D/A and A/D conversions. Uses an AUI device as the isolation barrier between the high-voltage phone line and the low-voltage modem DSP.	48-pin TQFP, line-powered, software-programmable silicon-based DAA.
Modem - Codec	CSP1037B (3 Volt)	Line codec for use with Agere's CSP1037 soft modem device.	CSP1037 chip set is an integrated DAA that provides a programmable line interface to meet international telephone line requirements. CSP1037B provides analog signal filtering along with D/A and A/D conversions. Uses capacitive coupling as the isolation barrier between the high-voltage phone line and the low-voltage modem digital interface circuitry.	16-pin SOIC and 16-pin TSSOP.
Modem - Codec	CSP1038 (3 Volt)	Line codec for use with a variety of Agere's modem devices.	Can frequently be used to reduce overall BOM costs for host-based, controllerless, and soft modem offerings.	16-pin SOIC.

Product Family	Product	Description	Function	Key Features/Benefits
Modem - Codec	T38 (3.3 Volt)	T38 is a sigma-delta audio codec with programmable sample rates from 7.2 through 11.25 kHz and is used in modem applications requiring telephone answering support (TAM) or speakerphone capabilities (FDSP).	Provides analog signal filtering along with D/A and A/D conversions with up to 40 dB of SNR.	T38 superceeds the former Agere CSP1027 and T7525 audio codecs and comes in 16-pin TSSOP. T38 features single-ended input/output for handset connection and differential input/output for quality audio circuits.
Modem - Controller-Based Venus®	1673 (5 Volt) 1675 (3 Volt) 1670 V.34 only	Controller-based analog client data/FAX modem - optimized for embedded applications.	Performs modem controller and data pump functionality in a single chip. Supports ITU recommended data rates up to and including V.92 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, V.21 Ch2, and V.34.	Interfaces to host controller using standard AT-command set with hardware interface support for RS232-TTL, ISA, PCMCIA, USB 1.1 (requires USS820-D device), and PCI 2.0 (requires PITA device). Packages: 128-pin TQFP and 144-pin TQFP. Software support for error correction: *MNP*®2-4 and V.42. Data compression: *MNP*5, V.42bis, and V.44. FAX capabilities: V.34, V.29, V.19, V.27ter, V.21 Ch2, and Class 1/Class 2. Enhanced voice features: full-duplex speakerphone capabilities and TAM. Excellent support for worldwide homologation. Interfaces to telephone line through a line codec such as CSP1034 or CSP1035A and DAA. V.92 not available with CSP1035A.
Modem - Controllerless	DSP1648C (3 Volt)	PCI-based controllerless analog client data/FAX modem ideal for *Windows*®/WinCE environments. Typically used in desktop and notebook computers as PCI cards, *MINI PCI*®, and PC cards.	DSP1648C performs modem data pump functionality while the host processor performs high-level modem (controller) protocol processing. Supports ITU recommended data rates up to and including V.92 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, and V.21 Ch 2.	DSP1648C interfaces to host controller using PCI bus interface. Low-power modes. Package: 100-pin TQFP. Software drivers are compliant with *Windows* 95, 98, 98SE, 2000, *Windows NT*® 4.0, *Windows ME*™, *Windows XP*™ OS support and provide support for error correction: *MNP*2-4 and V.42. Data compression: *MNP*5, V.42bis, and V.44. Enhanced voice features: full-duplex speakerphone capabilities and TAM. Excellent support for worldwide homologation. Interfaces to telephone line through a line codec such as CSP1034C or CSP1035A and DAA.
Modem - Core	DP2S	Synthesizable analog client modem data pump core for incorporation into an ASIC.	Digital functions of modem circuit can be integrated into a system ASIC. DAA/codec functionality remains as an external discrete part of the modem solution. Suitable integration path for high-volume applications as a low-cost, high-density modem implementation. Typical applications are set-top boxes (STB) and multifunction peripherals (MFPs).	Architecture is ASIC friendly and highly integratable into user-specified process technologies via industry-standard synthesis and simulation process flows. Flexible memory configuration provides various ITU data modulation rates (e.g., V.92, V.34, V.22) and FAX functionality, which is object code compatible with Agere's DP2 embedded modem family. PWM output for low-cost line monitoring and audio codec for TAM and FDSP in addition to compatibility with the CSP1034C or CSP1035A line codecs.
Modem - Embedded Controllerless	DP2LV34D DP2LV34X DP2LV17X DP2LV22D	Controllerless ISA-like analog client data/FAX modem. Optimized for small footprint and low-power embedded applications.	Performs modem data pump functionality while the host processor performs high-level modem (controller) protocol processing. Supports ITU recommended data rates up to and including V.34 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, V.21 Ch2, and V.34.	Cost reduced, footprint compatible to DP2Vxxx family. Interfaces to host controller using a 3.3 V 8-bit microcontroller (ISA-like) interface. Call progress speaker driver. Package: 48-pin TQFP. DP2LV34D supports V.34 data and V.17 FAX. DP2LV34X supports V.34 FAX. DP2LV17X supports V.17 FAX. DP2LV22D supports V.22bis data, optional V.42 error correction, V.42bis data compression, and V22 FC. Excellent support for worldwide homologation. Interfaces to telephone line through a line codec such as CSP1034 or CSP1035A and DAA.

Product Family	Product	Description	Function	Key Features/Benefits
Modem - Embedded Controllerless	DP2V90DX DP2V34DX DP2V34X DP2V32DX	Controllerless ISA-like analog client data/FAX modem. Optimized for small footprint and low-power embedded applications.	Performs modem data pump functionality while the host processor performs high-level modem (controller) protocol processing. Supports ITU recommended data rates up to and including V.92 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, V.21 Ch2, and V.34.	Interfaces to host controller using a 3.3 V 8-bit microcontroller (ISA-like) interface. Call progress speaker driver. Package: 48-pin TQFP. DP2V90DX supports V.92, V.90/V.34 data, and V.34/V.17/V.29 FAX. DP2V34DX supports V.34 data and V.17 FAX. DP2V34X supports V.34 FAX. DP2V32DX supports V.32bis data and V.17 FAX. Excellent support for worldwide homologation. Interfaces to telephone line through a line codec such as CSP1034 or CSP1035A and DAA.
Modem - One-Chip Modem	OCM-22 (3 Volt)	Low-speed analog modem. V.22bis modulation (2400 bits per second and lower).	Performs modem controller and data pump functionality in a single chip. Supports ITU recommended data rates up to and including V.22bis for use in very low-cost analog modem for use in point of sale terminals, set top box, etc.	48-pin TQFP package with serial interface to the host controller provides very low-cost V.22bis modem solution.
Modem - One-Chip Modem	OCM-34 OCM-92 (3 Volt)	High-speed analog modem.	Performs modem controller and data pump functionality in a single chip. Supports ITU recommended data rates up to and including V.90 with additional V.92 features: modem on hold and quick connect. Additionally supports new V.44 data compression scheme.	OCM-34 and OCM-92 support V.34 and V.92 data rates respectively. Both packages offer serial or parallel interfacing. OCM-92 is also offered in a 128-pin TQFP. This package option allows users to customize their firmware needs and also provides a path to connect the T-38 audio codec for voice applications.
Modem - Soft	CSP1037 (3 Volt)	AC97-based soft analog client data/FAX modem ideal for *Windows*/WinCE environments. Typically used in notebook computers using AC97 bus technologies for modem daughter/riser cards (MDC, AMR, CNR).	The host processor (e.g., *Pentium*) performs all modem data pump and controller functionality. Supports ITU recommended data rates up to and including V.92 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, and V.21 Ch 2.	Software drivers are compliant with *Windows* 98, 98SE, 2000, NT 4.0, *Windows ME, Windows XP* OS support. Package: 16-pin SOIC and 16-pin TSSOP. Worldwide DAA support. Interfaces to CSP1037B line-side device.
Modem - Soft	SV92A2 (3 Volt)	Dual mode—AC97 and HD audio (Azalia)—soft analog client data/FAX modem ideal for *Windows*/WinCE environments. Typically used in notebook computers using AC97/HD audio bus technologies for modem daughter/riser cards (MDC, AMR, CNR).	The host processor (e.g., *Pentium*) performs all modem data pump and controller functionality. Supports ITU recommended data rates up to and including V.92 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, and V.21 Ch 2.	SV92A2 interfaces to host controller using AC97 or HD audio bus interface. Package: 16 SOIC. PC2001/ACPI compliant. Software drivers are compliant with *Windows* 98, 98SE, 2000, NT 4.0, *Windows ME*, *Windows XP* OS support. Excellent support for worldwide homologation, as the same board can be used in both AC97 and HD audio environments without the need for recertification. Interfaces to telephone line through CSP1038 and DAA.

Product Family	Product	Description	Function	Key Features/Benefits
Modem - Soft	SV92PL (3 Volt)	PCI 2.2-based soft analog client data/FAX modem ideal for *Windows*/WinCE environments. Typically used in desktop and notebook computers as PCI and *MINI PCI* cards.	The host processor (e.g., *Pentium*) performs all modem data pump and controller functionality. SV92PL is a system-side device that interfaces to the host via a standard PCI or PCI 2.2 compliant bus. Supports ITU recommended data rates up to and including V.92 with legacy support for Bell 212A and Bell 103. Supports caller-ID (Bell 202 and V.23) and FAX mode capabilities: V.17, V.29, V.27ter, and V.21 Ch 2.	SV92PL interfaces to host controller using PCI 2.2 bus interface and is pin and footprint compatible with he DSP1648C device. Package: 100-pin TQFP. PC2001 compliant. Software drivers are compliant with *Windows* 95, 98, 98SE, 2000, NT 4.0, *Windows ME*, *Windows XP* OS support. Excellent support for worldwide homologation. Interfaces to telephone line through a line codec such as CSP1034C or CSP1035A and DAA.
Network Processor	*PayloadPlus* APP100	Full-featured, high-capacity ATM adaptation layer (AAL2) co-processor for the APP550/530 network processor devices.	Provides AAL2 SAR for 32K CIDs and 16K VCs. Supports AAL2 termination, generation, and AAL2 CPS switching. Maximum bandwidth = 622 Mbits/s.	Highest throughput and largest number of conversations of any AAL2 solution on the market.
Network Processor	*PayloadPlus* 600M APP310	600 Mbits/s single-chip network processor with available prevalidated software solutions for DSLAM, node B, and other access applications. Enables new revenue generating services for DSL, broadband, and wireless applications.	Provides easy to program multiservice traffic processing, including classification, traffic management, modification, SAR, OAM, statistics/billing. Supports comprehensive processing and interworking of Ethernet, ATM, IPv4/v6, MPLS, etc.	Industry-leading cost-power-performance. Rich set of integrated interfaces, including SPI-3, POS-PHY2, UTOPIA 3/2, and 10/100/1000 Ethernet. Sophisticated hierarchical scheduling/shaping. Integrated ARM-based control processor.
Network Processor	*PayloadPlus* 1.25G APP320	1.6 Gbits/s single-chip network processor with available prevalidated software solutions for DSLAM, node B, and other access applications. Enables new revenue generating services for DSL, broadband, and wireless applications.	Provides easy to program multiservice traffic processing, including classification, traffic management, modification, SAR, OAM, statistics/billing. Supports comprehensive processing and interworking of Ethernet, ATM, IPv4/v6, MPLS, etc.	Industry-leading cost-power-performance. Rich set of integrated interfaces, including SPI-3, POS-PHY2, UTOPIA 3/2, and 10/100/1000 Ethernet. Sophisticated hierarchical scheduling/shaping. Integrated ARM-based control processor.
Network Processor	*PayloadPlus* 2G APP340	2 Gbits/s single-chip network processor with available prevalidated software solutions for DSLAM, node B, and other access applications. Enables new revenue generating services for DSL, broadband, and wireless applications.	Provides easy to program multiservice traffic processing, including classification, traffic management, modification, SAR, OAM, statistics/billing. Supports comprehensive processing and interworking of Ethernet, ATM, IPv4/v6, MPLS, etc.	Industry-leading cost-power-performance. Rich set of integrated interfaces, including SPI-3, POS-PHY2, UTOPIA 3/2, and 10/100/1000 Ethernet. Sophisticated hierarchical scheduling/shaping. Integrated ARM-based control processor.
Network Processor	*PayloadPlus* 2.5G APP520	Highly integrated 2.5 Gbits/s network processors for Ethernet bridging, VLANs, Ethernet over SONET.	Programmable layer 2-4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Optimized for Ethernet and packet/frame processing at aggressive price points.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best-in-class traffic management. The APP520 integrates into the NP Ethernet MACs, full-featured traffic management, and a high-performance search engine.

Product Family	Product	Description	Function	Key Features/Benefits
Network Processor	*PayloadPlus* 2.5G APP530	Highly integrated 2.5 Gbits/s network processor for edge/access and multi-service applications.	Programmable layer 2–4 plus protocol processing, traffic management/ shaping/modification and policing & statistics. Designed for full multiservice internetworking of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line-rate performance, and best-in-class traffic management. The APP530 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured, multiservice-capable traffic management, and a high-performance search engine.
Network Processor	*PayloadPlus* 2.5G APP530TM	Highly integrated 2.5 Gbits/s network processors for edge/access and multi-service applications. These devices include prewritten software to perform ATM SARing, traffic management, policing, and OAM.	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Designed for full multiservice internetworking of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line-rate performance, and best-in-class traffic management. The APP530 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured, multiservice-capable traffic management, and a high-performance search engine.
Network Processor	*PayloadPlus* 5G APP540	Highly integrated 5 Gbits/s network processors for Ethernet bridging, VLANs, Ethernet over SONET.	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Optimized for Ethernet and packet/frame processing at aggressive price points.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line-rate performance, and best-in-class traffic management. The APP540 integrates into the NP Ethernet MACs, full-featured, traffic management, and a high-performance search engine.
Network Processor	*PayloadPlus* 5G APP550	Highly integrated 5 Gbits/s network processor for edge/access and multi-service applications.	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Designed for full multiservice internetworking of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line-rate performance, and best-in-class traffic management. The APP550 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured, multiservice-capable traffic management, and a high-performance search engine.
Network Processor	*PayloadPlus* 5G APP550TM	Highly integrated 5 Gbits/s network processors for edge/access and multi-service applications. These devices include prewritten software to perform ATM SARing, traffic management, policing, and OAM.	Programmable layer 2-4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Designed for full multiservice internet working of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line-rate performance, and best-in-class traffic management. The APP550 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured multiservice-capable traffic management, and a high-performance search engine.
Network Processor Software	APP5TMSARRTE-SW	Software package available for the APP550 network processors. Includes data-plane software that is validated on hardware using test cases that reflect system scenarios. It is used in conjunction with the APP5xx Object-API (RTE).	The APP550TM-SAR software package provides AAL5 SAR, TM4.1 traffic management, and I.610 ATM operations, administration, and maintenance (OAM) capabilities. These capabilities allow you to perform processor-intensive SAR, traffic management (TM), and OAM functions in a single device, off-loading other devices in the processing chain. Furthermore, because the APP550 is a fully functional network processor, flexibility can be built in for future system enhancements by modifying the software.	The ready-to-use, comprehensive application software and simplified control plane interface save equipment vendors several months of application development and system integration time, enabling rapid development of ATM-based systems.

Product Family	Product	Description	Function	Key Features/Benefits
Network Processor Software - DSLAM FPI Layer 2 Package	APP3FPIMDSLL2-SW - Modifiable Source License; APP3FPIMDSLL2-NSW - Non-modifiable License	DSLAM line card application software package for the APP3xx network processors supporting Layer 2 bridging models. Includes data-plane and control plane software with functional API (FPI) interfaces—at an abstraction layer above object-level API. Software is validated on hardware with APP300 and DSL modems and is available with non-modifiable (APP3FPIMDSLL2-NSW) or modifiable source license (APP3FPIMDSLL2-SW).	Targeted for Layer 2 IP DSLAM line card application with device-independent functional API. Comprehensive features include support for all four encapsulations (PPPoE, PPPoA, IPoE, and IPoA) , VLAN tagging and stripping, IGMP multicast, ATM TM and OAM, performance monitoring, statistics collection, and host-NP communication, etc. High degree of configurability. Makes the APP300 look like a "configurable" chip for DSLAM Layer 2 line card processing applications. Can be augmented with proprietary features.	The ready-to-use, comprehensive application software enables OEMs to develop DSLAM line cards with APP300 to save approximately four quarters in application development and system integration time (time-to-market benefit) and over 100 staff-months in resources (reduced cost of ownership). In addition, built-in customizability features enable customers with modifiable source license to add proprietary features easily and quickly.
Network Processor Software - DSLAM FPI Layer 2 + Layer 3 Package	APP3FPIMDSLL23-SW - Modifiable Source License; APP3FPIMDSLL23 NSW - Non-modifiable License	DSLAM line card application software package available for the APP3xx network processors supporting Layer 2 bridging and Layer 3 routing models. Includes data-plane and control plane software with functional API (FPI) interfaces—at an abstraction layer above object-level API. Software is validated on hardware with APP300 and DSL modems. Available with non-modifiable (APP3FPIMDSLL23NSW) or modifiable source license (APP3FPIMDSLL23-SW).	Targeted for IP DSLAM line card application for layer 2 bridging and layer 3 routing modules with device-independent functional API. Comprehensive features include support for all four encapsulations for both bridging and routing models (PPPoE, PPPoA, IPoE, IPoA), VLAN tagging and stripping, IGMP multicast, ATM TM and OAM, performance monitoring, statistics collection, IP routing, PPP termination, and host-NP communication. High degree of configurability. Makes the APP300 look like a "configurable" chip for IP DSLAM (Layer 2 and Layer 3) line card processing applications. Can be augmented with proprietary features.	The ready-to-use, comprehensive application software enables OEMs to develop DSLAM line cards with APP300 to save approximately six quarters in application development and system integration time (time-to-market benefit) and over 150 staff-months in resources (reducing cost of ownership). In addition, built-in customizability features enable customers with modifiable source license to add proprietary features easily and quickly.
Network Processor Software - Wireless Access FPI - ATM Backplane and ATM Backhaul	APP3FPIWLSAPAH-SW - Modifiable Source License; APP3FPIWLSAPAH NSW - Non-modifiable License	Wireless node B/BTS and RNC software package for the APP3xx network processors. Supports ATM backplane and backhaul applications. Includes data-plane and control plane software with functional API (FPI) interfaces—at an abstraction layer above object-level API. Software is validated on hardware with APP300 and APP100. Available with nonmodifiable (APP3FPIWLSAPAHNSW) or modifiable source license (APP3FPIWLSAPAH-SW).	Targeted for wireless node B/BTS and RNC system I/O card applications using ATM in both the backplane and the backhaul. Has device-independent functional API with comprehensive software support for Iub or Abis interfaces for wireless networks. Features include ATM AAL2, AAL5, cell switching, TM 4.1, ATM I.610 OAM, perf. monitoring, statistics, and host-NP communication. High degree of configurability. In conjunction with LLP API, FPI makes the APP300 look like a "configurable" chip for these NIC applications. Can be augmented with proprietary features.	The ready-to-use, comprehensive application software enables OEMs to develop node B NICs or RNC system I/O cards with APP300, APP100, and LLP to save 4-6 quarters in application development and system integration time (time-to-market benefit) and about 100 staff-months in resources (reducing cost of ownership). In addition, built-in customizability features enable customers with modifiable source license to add proprietary features easily and quickly.

Product Family	Product	Description	Function	Key Features/Benefits
Network Processor Software - Wireless Access FPI - IP Backplane and ATM Backhaul	APP3FPIWLSIPAH-SW - Modifiable Source License; APP3FPIWLSIPAHNSW - Non-modifiable License	Wireless node B/BTS and RNC software package for the APP3xx network processors. Supports IP (over Ethernet) backplane and ATM backhaul applications. Includes data-plane and control plane software with functional API (FPI) interfaces - at an abstraction layer above object-level API. Software is validated on hardware with APP300 and APP100. Available with non-modifiable (APP3FPIWLSAPIHNSW) or modifiable source license (APP3FPIWLSAPIH-SW).	Targeted for wireless node B/BTS and RNC system I/O card applications using ATM backhaul and IP backplane. Has device-independent functional API with comprehensive software support for Iub or Abis interfaces for wireless networks. Features include: ATM AAL2, AAL5, cell switching, TM 4.1, ATM I.610 OAM, perf. monitoring, statistics, ATM<->IP/UDP translation, IP frag/defrag support on the Ethernet backplane, host-NP communication, etc. High degree of configurability. In conjunction w/ LLP API, FPI makes the APP300 look like a "configurable" chip for these applications. Can be augmented with proprietary features.	The ready-to-use, comprehensive application software enables OEMs to develop node B NICs or RNC system I/O cards with APP300, APP100, and LLP to save 4-6 quarters in application development and system integration time (time-to-market benefit) and about 100 staff-months in resources (reducing cost of ownership). In addition, built-in customizability features enable customers with modifiable source license to add proprietary features easily and quickly.
Printing & Imaging	PI301	Controller for monochrome inkjet and thermal FAX applications. Used in conjunction with Agere's CSP1034S modem codec.	The PI301 is a highly integrated controller that includes an *ARM*946, and two PPIO controllers and Agere's DP2S. It performs the functions of several controllers/discrete ICs in a single package including V.17 modem data pump, inkjet cartridge control, image scanning, A/D for analog front end, firmware-based image processing, paper-stepper control, and paper-feed control.	High level of integration in the PI301 enables FAX designers to significantly reduce total system BOM. It allows for systems to be built with a single external FLASH memory as opposed to the multiple external memories found on most FAX machines. The inclusion of programmable DP2S core enables FAX data pump feature enhancement via firmware. The *ARM*946, which runs at 160 MHz, has additional processing headroom that allows customers to differentiate their products by adding features via firmware. PCB design is greatly simplified by removing the need for multiple ICs.
Satellite Digital Audio Radio Service	Satellite Digital Audio Radio Chip Set	Agere designs, develops, and supplies a complete chip-level solution for decoding satellite digital audio radio service technology to radio manufacturers.	The satellite digital audio radio service solution supports two key elements: broadcast/content and receivers. The system employs time, frequency, and space diversity to provide service continuity. Service is by a *Sirius Satellite Radio*™ subscription with the capability for selective tiered service.	*Sirius Satellite Radio* controls the broadcast where they transmit an unparalleled selection of digital-quality 100% commercial-free music, plus sports, news, and telematics data to mobile receivers via direct broadcast satellites supplemented by gap filler terrestrial networks. *Sirius* is one of two companies licensed to provide digital satellite radio in the U.S.
Storage Disk Drive Electronics	Hard Disk Controller & Interface Technology	Disk controller ASICs.	The hard disk controller manages the job of transferring data between the HDD and host during read and write operations. Its servo logic is responsible for managing the position of heads during seeks (moving from one track to a nonadjacent track) and during tracking (staying on a single track). Agere supports all data interface standards: parallel ATA, serial ATA, SCSI, serial attached SCSI, and fiber channel. The controller logic and firmware is typically customer-owned IP.	Agere's hard disk controller IP is tailored for the design needs of portable consumer electronics and complements Agere's ultra-low-power read channels for integration in turnkey storage SoCs. Manufacturers lacking in-house controller design expertise or looking to speed their entry into new market segments can take advantage of Agere's complete storage controller solution. Agere also continues to serve HDD OEMs possessing their own proprietary controller technology (logic and firmware) by integrating their IP with interface PHYs to produce final silicon. Agere offers a complete line of interface PHYs for parallel standards (PATA, SCSI), serial standards (SATA, SAS, and FC), and consumer-based standards (MMC, CompactFlash, and CE-ATA), delivering robust designs for secure, high-speed data transfers between disk drives and host devices.

Product Family	Product	Description	Function	Key Features/Benefits
Storage Disk Drive Electronics	SoCs	Systems-on-a-chip.	SoCs integrate the functionality of the read channel, hard disk controller, servo logic, microprocessor, and memory on a single piece of silicon.	Agere's SoCs simplify disk drive design, improve reliability, reduce power consumption, and ease manufacturing without increasing drive costs. Agere provides a high-performance read channel, hard disk controller, high-density embedded memory, and broad selection of mixed-signal cores and I/O cells, plus the necessary IP, all implemented in state-of-the-art process technologies. Agere is the leading provider of highly integrated SoC solutions for the HDD industry.
Storage Disk Drive Electronics	*TrueStore* Motor Controllers	Motor controller ICs.	The motor controller drives the spindle motor that spins the disk drive platters and maintains the spin rate (RPMs). It also drives the voice coil motor (VCM) that moves the head gimbal assembly (HGA) from track to track during seek operations and then holds the HGA on-track during read and write operations.	Agere's motor controllers enable manufacturers to reach higher levels of integration and performance. On-chip power drivers help disk drive manufacturers cut product design time and manufacturing costs. Agere has engineered several features enabling improved reliability and shock resistance while minimizing additional external components.
Storage Disk Drive Electronics	*TrueStore* Preamplifiers	Preamplifier ICs.	As a drive reads a signal from the disk drive platter, the preamplifier is used to amplify minute analog signals before they are sent to a read-channel IC for digitization. Another function is to amplify data from the read channel for the drive head to write on the platter. Agere's preamps help protect the drive head from electrical voltage overstresses that typically occur during power mode transitions and magnetic interference by providing a balanced differential writer.	Agere's preamplifiers support high data rates and HDD best-in-class read-to-write recovery and noise performance. Agere uses the latest process technology to deliver superior performance. The combination of Agere's preamplifier ICs and read channels provides hard disk drive manufacturers with a very reliable data path and ensures the continued development of high-performance, high-capacity disk drives.
Storage Disk Drive Electronics	*TrueStore* Read Channels	Read channel ICs.	The read channel encodes and decodes the data going to/from the preamplifier. The read channel detects bits in analog signal form from the preamplifier and coverts them into digital form. Read channels use advanced mixed-signal and digital-signal processing technologies, in addition to advanced data-encoding schemes and digital filtering to optimize data detection. They are also involved in writing servo data during self-servo write operations and decoding servo information used for positioning drive heads during seeking and tracking operations.	Agere's *TrueStore* read channels enable high areal density through superior signal-to-noise ratio (SNR) performance. Agere uses CMOS technology to provide additional signal processing capabilities while maintaining small chip size and low power consumption. Agere offers numerous benefits for hard drive developers to improve capacity, ensure signal integrity, and lower manufacturing costs through repeatable run-out improvement, self-servo write capability, and perpendicular recording support. Agere's proven read channel technology, integration expertise, and broad portfolio of disk drive electronics provides customers with the capability to deliver high-performance storage products.

Product Family	Product	Description	Function	Key Features/Benefits
Switch Fabric	ASX/ACE	Multidevice 40 x 40 port ATM switch fabric solution. The ASX is the 8 x 8 port queuing, buffering, and arbitration device. The ACE is the 8 x 8 port crossbar device.	Switches 25 Gbits/s of ATM cell traffic in a 40 x 40 port matrix with user bandwidth of 622 Mbits/s per port. Seamlessly interconnects to the APC port managers.	25 Gbits/s user capacity. Eight 800 Mbits/s I/O ports. Nonblocking, loss-less, and self-routing switch fabric. No external memory required. Internal 512 cell size buffer. Four traffic classes. Fabric redundancy supported. 16-bit asynchronous µP interface.
Switch Fabric	BCST1A	Single-device 8 x 8 port ATM switch fabric solution.	Switches 5 Gbits/s of ATM cell traffic in an 8 x 8 port matrix with user bandwidth of 622 Mbits/s per port. Seamlessly interconnects to the APC port managers.	5 Gbits/s user capacity. Eight 800 Mbits/s I/O ports. Nonblocking and loss-less switch. No external memory required. Internal 512 cell size buffer. Four traffic classes. Fabric redundancy supported. 16-bit asynchronous µP interface.
TDM Interconnect	*Ambassador* T8100A	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 1024 time slots (TSs) between 16I/16O streams and 256 time slots to 32 bidirectional backplane streams providing clock mastering capabilities to the system.	1024 local TS capacity. 256 TS backplane capacity. 16I/16O local streams. 32 bidirectional backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching.
TDM Interconnect	*Ambassador* T8102	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 512 time slots (TSs) between 16I/16O streams and 32 bidirectional backplane streams providing clock mastering capabilities to the system.	512 TS backplane capacity. 16I/16O local streams. 32 bidirectional backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching.
TDM Interconnect	*Ambassador* T8105	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 1024 time slots (TSs) between 16I/16O streams and 512 time slots to 32 bidirectional backplane streams providing clock mastering capabilities to the system.	1024 local TS capacity. 512 TS backplane capacity. 16I/16O local streams. 32 bidirectional backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching.
TDM Interconnect	*Ambassador* T8110	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 4096 time slots (TSs) between 64 bidirectional local and backplane streams providing clock mastering capabilities to the system.	4096 local or backplane TS capacity. 64 bidirectional local and backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s or 16 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching. PCI or µP I/F.
Time-Slot Interchanger	TTSI1K	1k x 1k DS0 time-space-time TDM switch.	Switches 1024 time slots (TSs) between 16 Tx/Rx stream pairs.	1024 TS capacity. 16 Tx/16 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching. Test pattern generation. Output enables for Tx streams. Frame integrity/low-latency mode. 8-bit asynchronous µP I/F.
Time-Slot Interchanger	TTSI2K	2k x 2k DS0 time-space-time TDM switch.	Switches 2048 time slots (TSs) between 32 Tx/Rx stream pairs.	2048 TS capacity. 32 Tx/32 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching. Test pattern generation. Output enables for Tx streams. Frame integrity/low-latency mode. 8-bit asynchronous µP I/F.
Time-Slot Interchanger	TTSI4K	4k x 4k DS0 time-space-time TDM switch.	Switches 4096 time slots (TSs) between 32 Tx/Rx stream pairs.	4096 TS capacity. 32 Tx/32 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1-, 2-, or 4-bit subrate switching. Test pattern generation. Output enables for Tx streams. Frame integrity/low-latency mode. 8-bit asynchronous µP I/F.

Product Family	Product	Description	Function	Key Features/Benefits
Time-Slot Interchanger	TSI-8	8k x 8k DS0 time-space-time TDM switch.	Switches 8192 time slots (TSs) between 32 Tx/Rx stream pairs.	8192 TS capacity. 32 Tx/32 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s, or 16 Mbits/s. Test pattern generation/monitoring. 16 translation table look-ups. Frame integrity/low-latency mode. 16-bit synchronous µP I/F.
Time-Slot Interchanger	STSI-48	Scalable TSI. 48k x 16k linearly expandable to 48k x 48k using three devices.	The STSI-48 TSI is a 48k x 16k non-blocking time-slot (DS0) switch for use with serial TDM data streams. Typically used in central office TDM switches, DLLs, digital cross connects, remote access concentrators with voice/IP, and multiservice access platforms.	49152 x 16384 TS capacity. Nonblocking, 16 HSLs operating at an STS-12 data rate using pseudo-SONET framing, each transporting 81192 time slots between STSI-48 devices. Data rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s, and 16 Mbits/s. Frame integrity/low-latency mode. 16 translation table look-ups. Test pattern generation monitoring. Low power with 1.5 V core power supply and 3.3 V digital I/O compatibility.
Time-Slot Interchanger	STSI-144	Scalable TSI. 144k x 16k asymmetric DS0 time-space-time TDM switch.	Switches 16384 time slots (TSs) between 64 Tx/Rx stream pairs and 16 Tx/Rx high-speed serial link (HSL) pairs. Allows centralized and distributed 10G TDM switching.	147456 x 16384 TS capacity. 64 Tx/64 Rx TDM streams. 16 Tx/16 Rx HSL LVDS links (622 Mbits/s). Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s, or 16 Mbits/s. Test pattern generation/monitoring. 16 translation table look-ups. Frame integrity/ low-latency mode. 16-bit synchronous µP I/F.
TRAU	Link Layer Processor	Transcoder/rate adapter unit (TRAU) for use in 2G and 2.5G systems.	Termination of TRAU frames for 512 subchannels (full rate 16 kbit/s and half rate 8 kbit/s).	TRAU frames are carried at the Abis interface (between the BTS and the BSC). TRAU frames carry voice and control information in a GSM network.
TrueAdvantage Converged Access Solutions	*TrueAdvantage* Converged Access Solutions	A completely integrated set of hardware and software components for wireline and wireless service providers to expand their product offerings, generate higher revenues, and reduce their costs in the global battle to provide converged access services to consumers.	*TrueAdvantage* solutions function as a launching pad for telecommunications equipment manufacturers and service providers to rapidly create and deliver numerous revenue-generating services to any network at higher performance levels and lower costs than alternative technologies.	*TrueAdvantage* access solutions consist of five critical and inter-related elements: feature-rich networking chips, robust software development tools, integrated hardware development systems, proven reference designs developed, and turnkey application software. *TrueAdvantage* solutions enable the wireline and wireless access equipment industry to substantially reduce product development costs while accelerating equipment deliveries supporting new services by up to two years. By presenting a development framework unmatched in its ease of use and completeness, Agere is enabling customers to minimize not only initial development costs, but also future costs and time to market.
Unbreakable Access Technology	*Unbreakable Access* Technology	Combined hardware and software solution for improved network resiliency enabling the reliable delivery of value-adding, packet-based services.	Agere's *Unbreakable Access* technology is applied in conjunction with its network processor devices and offers selective IP service-level flow protection and ultra-fast restoration. *Unbreakable Access* provides a means to guarantee near hitless reliability of high-value IP services traffic across independent paths through the network. *Unbreakable Access*, working at the IP services layer, provides an extremely cost and bandwidth efficient way to offer guaranteed premium services across large packet networks.	Improved ability to deliver on cost-effective service reliability guarantees for premium IP service requirements. Extremely fast restoration times when compared with other packet-based solutions, scalable to a variety of IP service applications and line rates. Agere continues to offer and develop the capability of this key technolgy for providing the next generation of IP network reliability for traditional services such as VoIP, as well as next-generation industry-changing services like IP multimedia streaming and pseudowire.

Product Family	Product	Description	Function	Key Features/Benefits
Universal Serial Bus (USB)	USS-820D USS-820FD	USB 1.1 device controller.	USB 1.1 device controller with integrated transceiver provides a programmable bridge between USB and local microprocessor buses. It is programmable through a simple read/write register interface that is compatible with industry-standard microcontrollers.	Full compliance with USB 1.1. Self-powered or bus-powered USB device. Full-speed USB 1.1 operation (12 Mbits/s). Protocol control and administration for up to 16 USB endpoints (8 bidirectional endpoints). Supports USB remote wake-up feature. Glueless interface to microprocessor buses. 5 V tolerant I/O buffers allow operation in 3 V or 5 V system operation. Package: USS-820D—44-pin MQFP, USS-820FD—48-pin TFSBGA.
Wireless VoIP Phone Solutiont	WV8307	802.11-based wireless IP phone solution and reference design.	Low power consumption 802.11-based wireless IP phone for transmitting and receiving voice over a wireless LAN.	Complete solution using Agere ICs in a cell phone sized reference design. Comprised of T8307, CSP8307, WL60010 (or WL60011), and WL1141 MCM. Li-ION battery-powered platform features extended talk and standby time. Includes software (G.711 (annex I and II), G.729AB, G.723.1, G.726 & G.722 voice coders from Agere). Supports three-way conferencing. Software run-time licenses included.