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(B) Bias Circuits

Table 1 shows the maximum allowable gate current for each of NEC's high power GaAs FETS. Care should be taken at all times when planning bias circuits and input power to ensure that these values are not exceeded.

NE8001	3.0 mA
NE8002	6.0 mA
NE8004	10.0 mA
NE8008	15.0 mA
NE3716	20.0 mA
NE9000	0.5 mA
NE9001	1.3 mA
NE9002	2.6 mA
NE9004	5.0 mA
NE9008	8.0 mA
NE8681	3.0 mA
NE8682	6.0 mA
NE8684	10.0 mA
NE8688	15.0 mA
NE8691	1.3 mA
NE8692	2.6 mA
NE8694	5.0 mA

Table 1: Maximum Allowable Gate Currents for the NEC Power GaAs FET Series

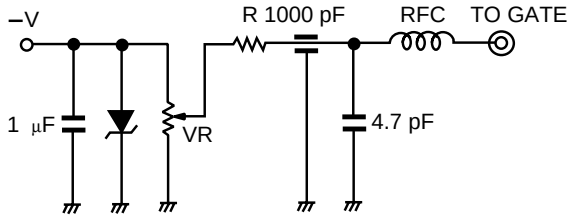

Figure 29. Example of a Gate Bias Circuit

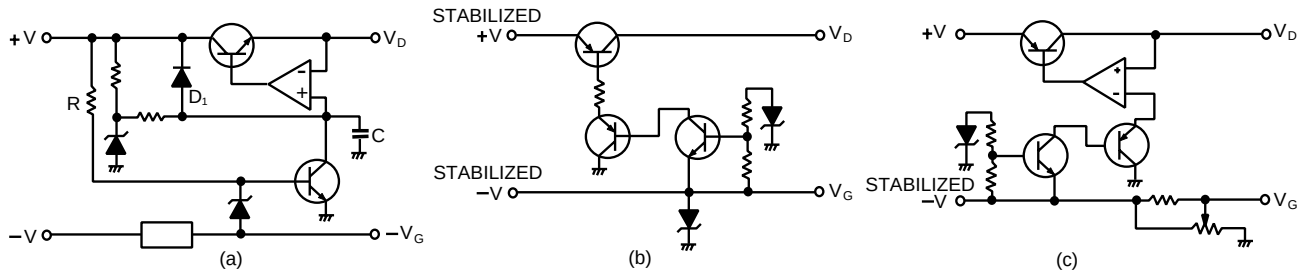

Figure 30. Power GaAs FET Bias Circuits

One thing that is very basic when biasing power GaAs FETs is the need for increased impedance of the gate bias circuit. The example in Figure 29 shows a type of feedback circuit incorporating a resistor in series with the bias circuit which produces a drop in potential when the current across the gate begins to increase, and adds to the gate series bias. By inserting a low pass filter, such as an RFC or capacitor, unnecessary oscillation or phase shift will be prevented.

Another important factor is the order in which bias is applied. It is generally disadvantageous, both thermally and electrically, to self-bias a power GaAs FET. Therefore, a positive and negative dual power source should be used to bias the drain and gate separately. For a GaAs FET, maximum current will flow when the gate voltage is at zero. With a high output level FET, I_{DSS} is sometimes greater than several amps and since typical g_m is extremely high, oscillation will occur and the FET will be destroyed either thermally or electrically. For this reason, any appreciable flow of high current must be prevented from reaching the drain. The bias method used must be one whereby negative voltage is applied to the gate first, after which positive voltage is applied to the drain. The following is a detailed example of this method.

(1) Add a negative potential to the gate which is close to -5V or to the pinch off voltage.

(2) Specify the drain voltage in such a way that it moves as rapidly and smoothly as possible from zero volts to the preset V_D. If there is no possibility of a surge voltage being produced and the drain voltage is completely stable, add the preset voltage instantaneously.

Figure 30 gives three recommended bias circuits for biasing power FETS. Figure 30(a) is an excellent bias circuit because there are no limitations requiring that either positive or negative voltage be applied to the circuit first. Drain voltage, V_D, will reach its preset value according to the time