



电子元器件系列 (中国.厦门)

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W24010/LL

128K × 8 CMOS STATIC RAM

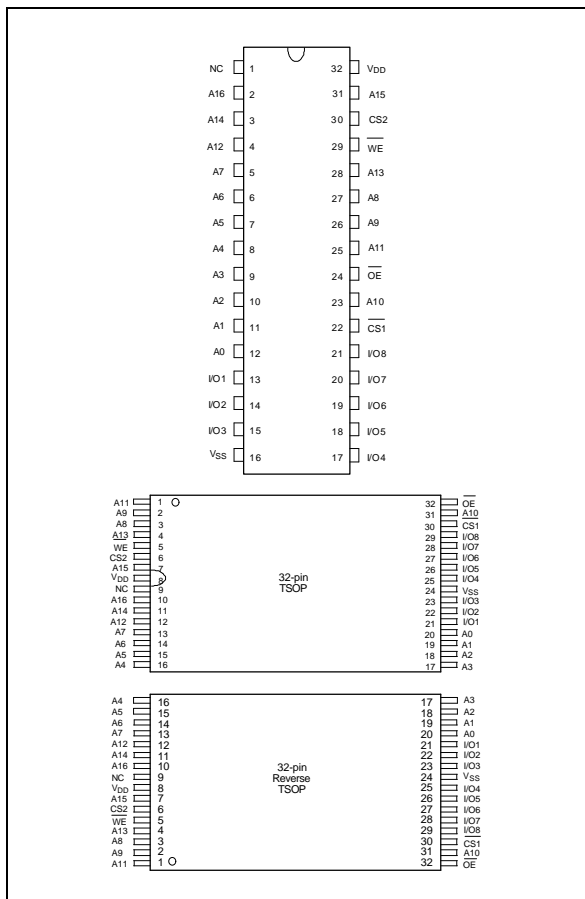
GENERAL DESCRIPTION

The W24010 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

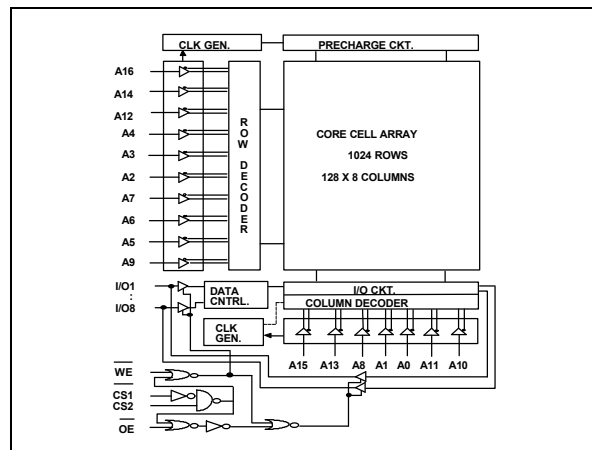
FEATURES

- Low power consumption:
 - Active: 350 mW (max.)
 - Standby: 250 μW (max.)
- Access time: 70 nS (max.)
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 32-pin 600 mil DIP, 450 mil SOP, standard type one TSOP (8 mm × 20 mm), reverse type one TSOP (8 mm × 20 mm), small type one TSOP (8 mm × 13.4 mm) and reverse small type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

$\overline{CS1}$	CS2	\overline{OE}	\overline{WE}	MODE	I/O1–I/O8	V _{DD} CURRENT
H	X	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
X	L	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	H	Output Disable	High Z	I _{DD}
L	H	L	H	Read	Data Out	I _{DD}
L	H	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to 70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-	+2.2	-	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-1	-	+1	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{CS} = V_{IH}$ (min.) or $\overline{OE} = V_{IH}$ (min.) or $\overline{WE} = V_{IL}$ (max.)	-1	-	+1	μA
Output Low Voltage	V _{OL}	I _{OL} = +2.1 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	-	-	V
Operating Power Supply Current	I _{DD}	$\overline{CS} = V_{IL}$ (max.), I/O = 0 mA, Cycle = min. Duty = 100%	-	-	70	mA
Standby Power Supply Current	I _{SB}	$\overline{CS} = V_{IH}$ (min.), Cycle = min. Duty = 100%	-	-	3	mA
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	50	μA

CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

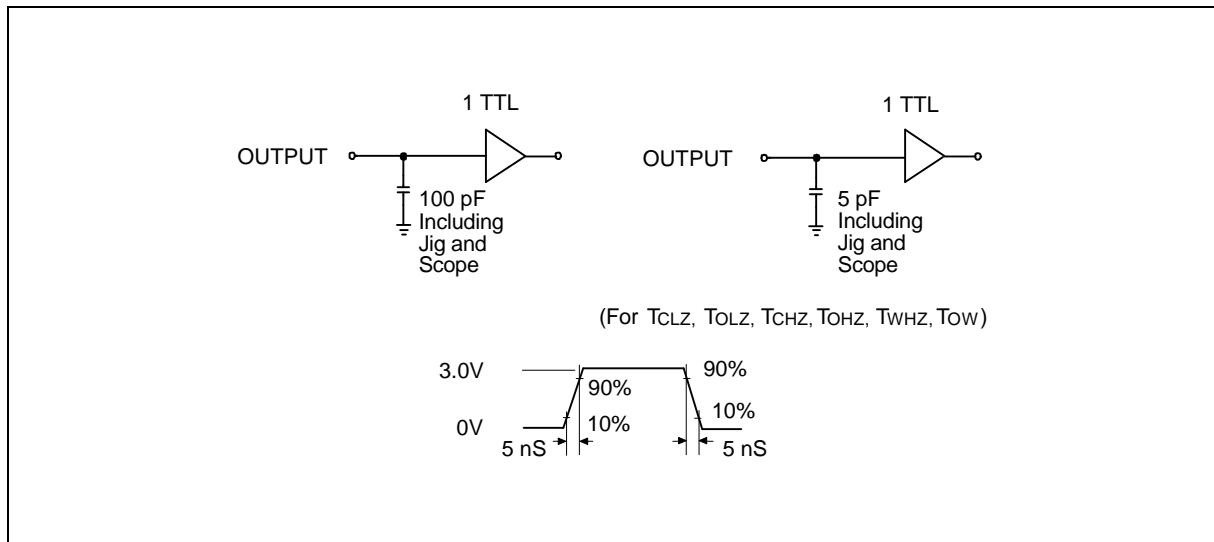
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

Read Cycle

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	T _{RC}	70	-	nS
Address Access Time	T _{AA}	-	70	nS
Chip Select Access Time	T _{ACS}	-	70	nS
Output Enable to Output Valid	T _{AOE}	-	35	nS
Chip Selection to Output in Low Z	T _{CLZ} *	10	-	nS
Output Enable to Output in Low Z	T _{OLZ} *	5	-	nS
Chip Deselection to Output in High Z	T _{CHZ} *	-	30	nS
Output Disable to Output in High Z	T _{OHZ} *	-	30	nS
Output Hold from Address Change	T _{OH}	10	-	nS

*These parameters are sampled but not 100% tested

Write Cycle

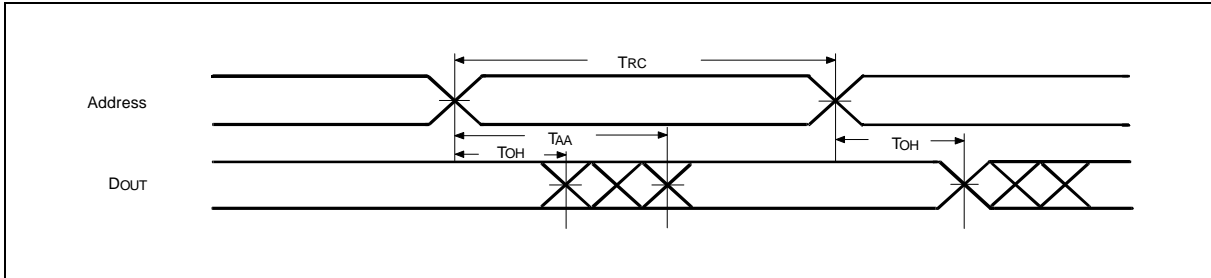
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	T _{WC}	70	-	nS
Chip Selection to End of Write	T _{CW}	50	-	nS
Address Valid to End of Write	T _{AW}	50	-	nS
Address Setup Time	T _{AS}	0	-	nS
Write Pulse Width	T _{WP}	50	-	nS
Write Recovery Time	$\overline{CS1}, CS2, \overline{WE}$	0	-	nS
Data Valid to End of Write	T _{DW}	30	-	nS
Data Hold from End of Write	T _{DH}	0	-	nS
Write to Output in High Z	T _{WHZ} *	-	25	nS
Output Disable to Output in High Z	T _{OHZ} *	-	25	nS
Output Active from End of Write	T _{OW}	5	-	nS

*These parameters are sampled but not 100% tested

TIMING WAVEFORMS

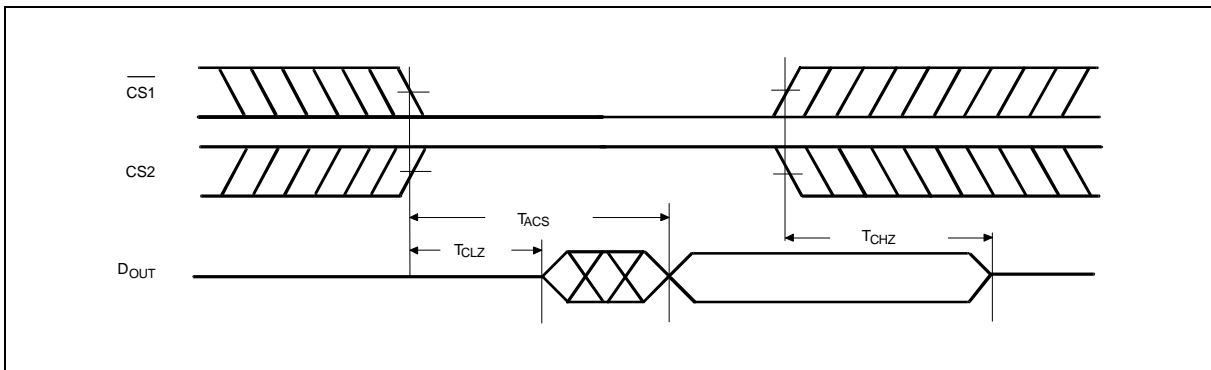
Read Cycle 1

(Address Controlled)



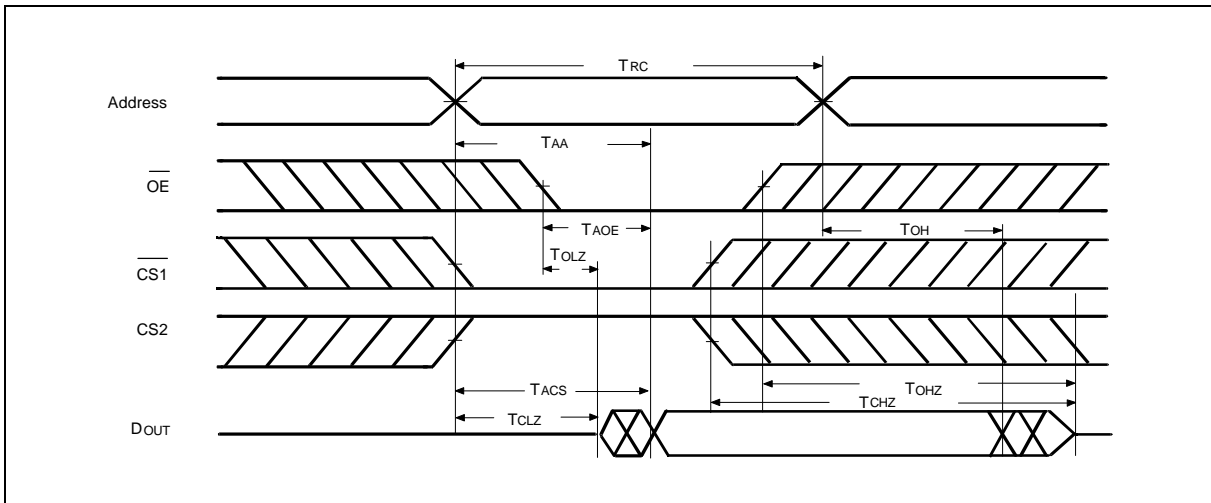
Read Cycle 2

(Chip Select Controlled)



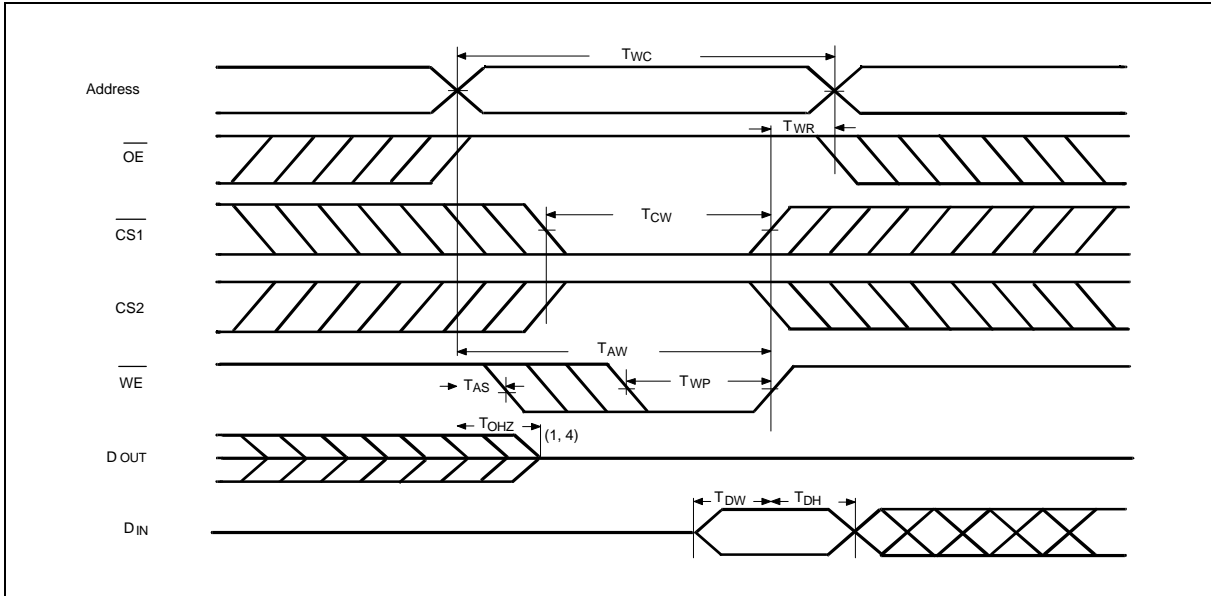
Read Cycle 3

(Output Enable Controlled)



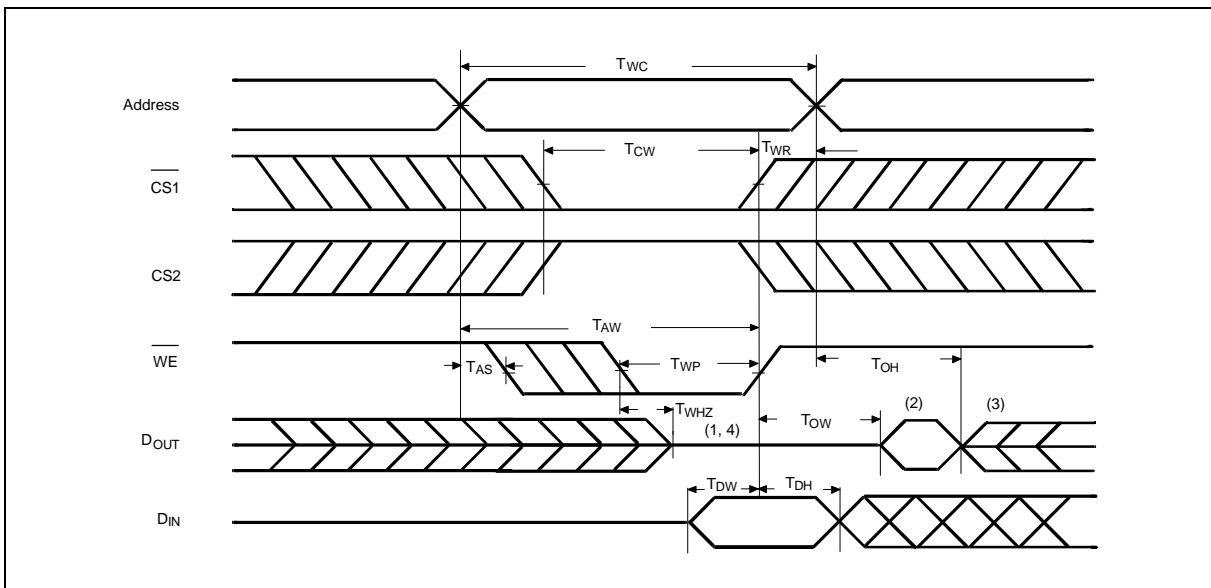
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

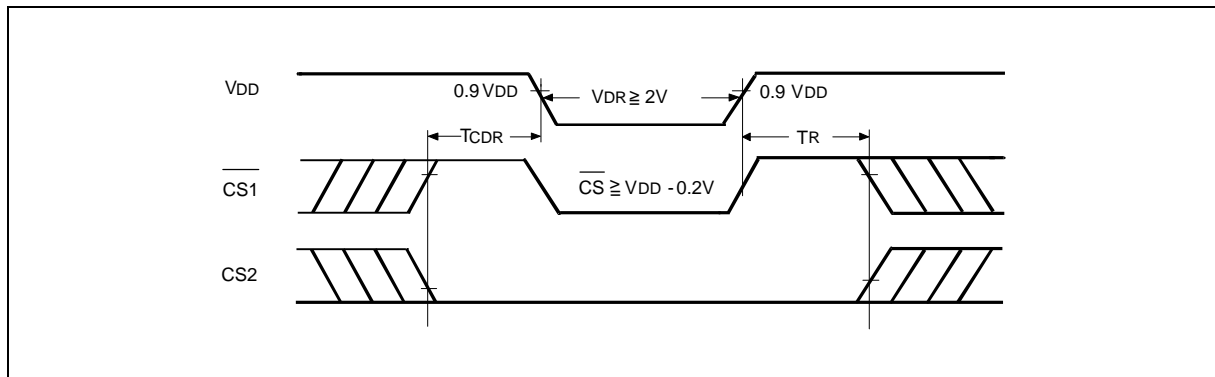
DATA RETENTION CHARACTERISTICS

(TA = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS} \geq V_{DD} - 0.2V$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS} \geq V_{DD} - 0.2V, V_{DD} = 3V$	-	-	20	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



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ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μ A)	PACKAGE
W24010-70LL	70	70	50	600 mil DIP
W24010S-70LL	70	70	50	450 mil SOP
W24010T-70LL	70	70	50	Standard type one TSOP
W24010U-70LL	70	70	50	Reverse type one TSOP
W24010Q-70LL	70	70	50	Small type one TSOP
W24010V-70LL	70	70	50	Reverse small type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.